



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Matthew J. Adiletta      Art Unit: 2183  
Serial No.: 10/615,500              Examiner: Richard L. Ellis  
Filed : July 8, 2003              Assignee: Intel Corporation  
Title : PARALLEL PROCESSOR ARCHITECTURE

**MAIL STOP RCE**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicant calls attention to the attached Information Disclosure Statement and documents listed on form PTO-1449.

This filing is being made before the receipt of a first Office action on the merits of the Request for Continued Examination. No fee is required.

The documents are in the English language; hence no concise explanation is necessary per Rule 98(a)(3).

Consideration of the foregoing and enclosures plus the return of a copy of the enclosed form PTO-1449 with the

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

February 22, 2006

Date of Deposit

Signature

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Certificate

Examiner's initials in the left column per MPEP 609 are earnestly solicited along with an early action on the merits.

Please apply any other charges or credits to deposit account 06-1050, referencing attorney docket 10559-075002.

Respectfully submitted,

Date:

Feb. 22, 2006

Ido Rabinovitch

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Reg. No. L0080

Atty. for the Intel Corporation

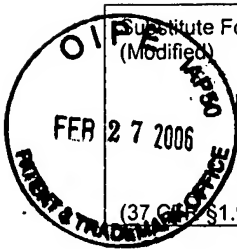
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 Substitute Form PTO-1449  
 (Modified)

 U.S. Department of Commerce  
 Patent and Trademark Office

 Attorney's Docket No.  
 10559-075002

 Application No.  
 10/615,500

**Information Disclosure Statement  
 by Applicant**

(Use several sheets if necessary)

(37 C.F.R. § 1.98(b))

 Applicant  
 Matthew J. Adiletta

 Filing Date  
 July 8, 2003

 Group Art Unit  
 2183

**U.S. Patent Documents**

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	2004/0148382	07/29/04	Narad et al.			
	AB	2004/0109369	6/10/2004	Wolrich et al.			
	AC	2004/0098496	5/20/2004	Wolrich et al.			
	AD	2004/0073728	4/15/2004	Wolrich et al.			
	AE	2004/0071152	4/15/2004	Wolrich et al.			
	AF	2004/0054880	3/18/2004	Bernstein et al.			
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	AH	3,736,566	5/29/1973	Anderson et al.			
	AI	4,709,347	11/24/1987	Kirk, David L.			
	AJ	4,890,218	12/26/1989	Bram			
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	AL	5,404,464	4/4/1995	Bennett			
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	AN	5,459,843	10/17/1995	Davis			
	AO	5,485,455	1/16/1996	Dobbins et al.			
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	AT	5,768,528	6/16/1998	Stumm			
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	BA	6,032,190	2/29/2000	Bremer et al.			

Examiner Signature

Date Considered

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-075002	Application No. 10/615,500
<b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Matthew J. Adiletta	
		Filing Date July 8, 2003	Group Art Unit 2183

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	BB	6,067,300	5/23/2000	Baumert et al.			
	BC	6,141,677	10/31/2000	Hanif et al.			
	BD	6,272,520	8/7/2001	Sharangpani et al.			
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	BZ	6,983,350	1/3/2006	Adiletta et al.			

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		Filing Date July 8, 2003	Group Art Unit 2183

Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	CA	WO 01/16718	3/8/2001	WIPO				
	CB	WO 03/030461	4/10/2003	WIPO				

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	CC	Chandranmenon, G.P. et al., "Trading Packet Headers for Packet Processing," IEEE/ACM Transactions on Networking 4(2): 141-152 (April 1996)
	CD	Dictionary of Computer Words: An A to Z Guide to Today's Computers, Revised Edition, Houghton Mifflin Company: Boston, Massachusetts, pp. 220, (1995)
	CE	Digital Semiconductor 21140A PCI Fast Ethernet LAN Controller, Hardware Reference Manual, Digital Equipment Corporation, pages i-x, 1-1 through 1-5, 2-1 through 2-12, 3-1 through 3-38, 4-31 through 5-2, 6-1 through 6-24, (March 1998)
	CF	News.Com, August 26, 1999. "Enterprise Hardware, Intel Expected to Unveil New Networking Chip," <a href="http://new.com.com/Intel+expected+to+unveil+new+networking+chip/2100-1001_3-230315.html">http://new.com.com/Intel+expected+to+unveil+new+networking+chip/2100-1001_3-230315.html</a> (accessed on 08/23/05), pages 1-5

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